Orientation of the Lab course

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Experiments in the Lab Course

- The use of Plastic Scintillators as “trigger counters”

- FPGA understanding using the DE2 Kit

Plastic Scintillator Lab

- Plastic Scintillators with PMT Readout

(As cosmic muon trigger counters)

- The choice of the electronic modules in HEP experiments (HV supply,scalers,logic units)
- A Mini Data Acquistion Setup using only handful of modules
- Efficiency of the scintillator counter

What is a **F**ield **P**rogrammable **G**ate **A**rray ?

A quick answer for the impatient

- An FPGA is an integrated circuit
- Mostly digital electronics
- An FPGA is programmable in the field (=outside the factory), hence the name “field programmable”
- Design is specified by schematics or with a hardware description language
- Tools compute a programming file for the FPGA
- The FPGA is configured with the design
- Your electronic circuit is ready to use
- With an FPGA you can build electronic circuits …
- … without using a soldering iron
- … without plugging together existing modules
- without having a chip produced at a factory

The building blocks: logic gates

Truth table

AND gate

INPUT		OUTPUT
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

C equivalent
q = a && b;

OR gate

INPUT		OUTPUT
A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

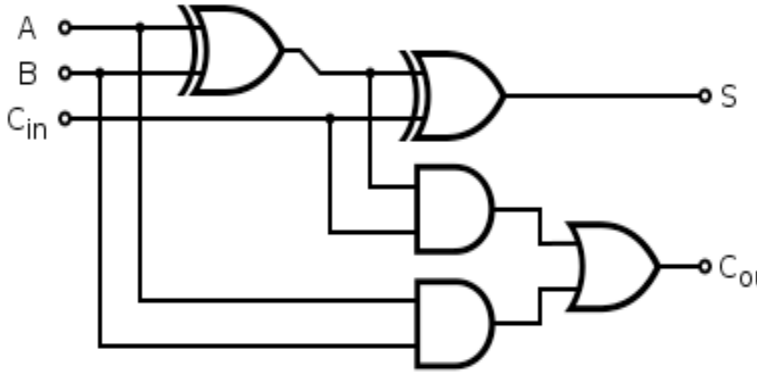
q = a || b;

XOR gate

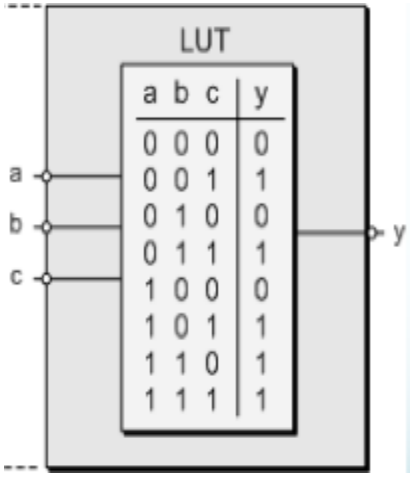
INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

q = a != b;

Combinatorial logic (asynchronous)

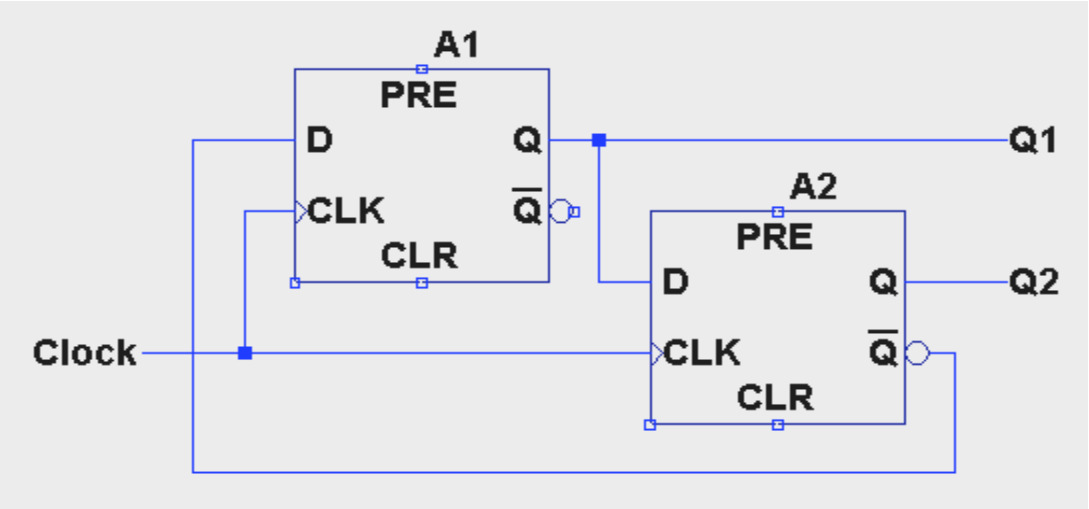


Outputs are determined by Inputs, only



Combinatorial logic may be implemented using Look-Up Tables (LUTs)

(Synchronous) sequential logic



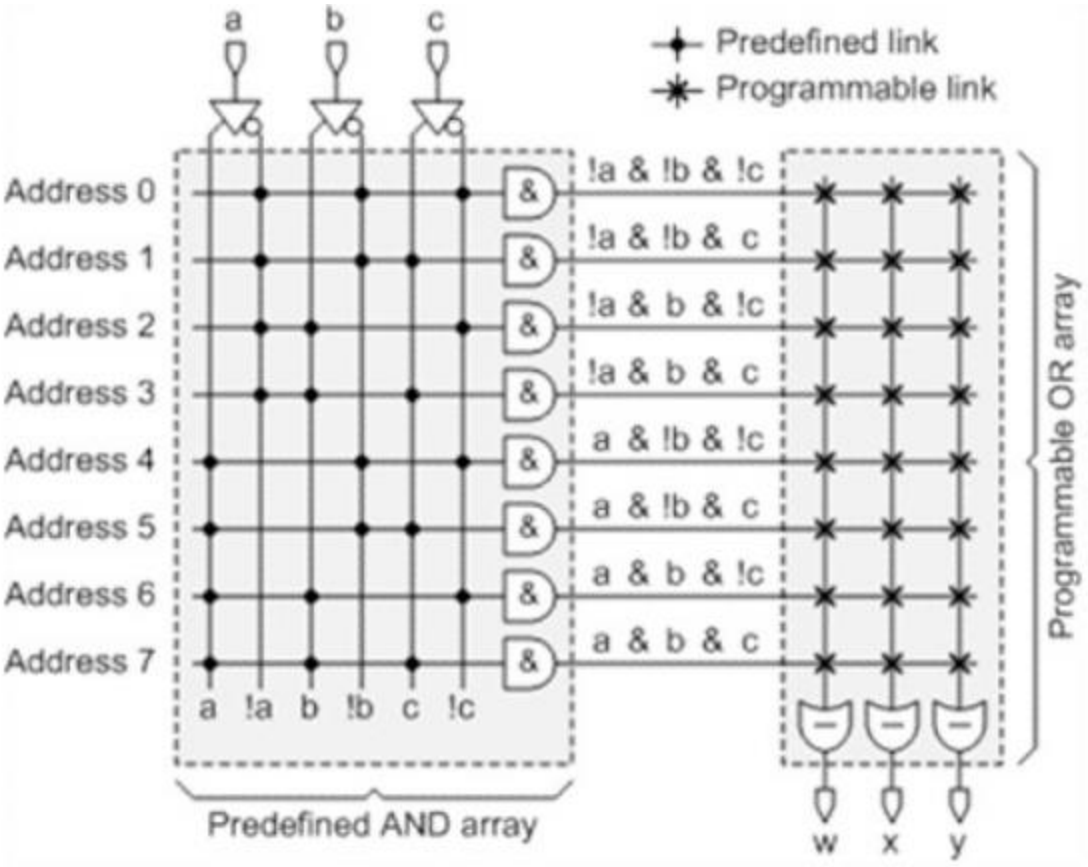
2-bit binary counter

Outputs are determined
by Inputs and their History
(Sequence)
The logic has an internal state

Using Look-Up-Tables and Flip-Flops
any kind of digital electronics may be implemented

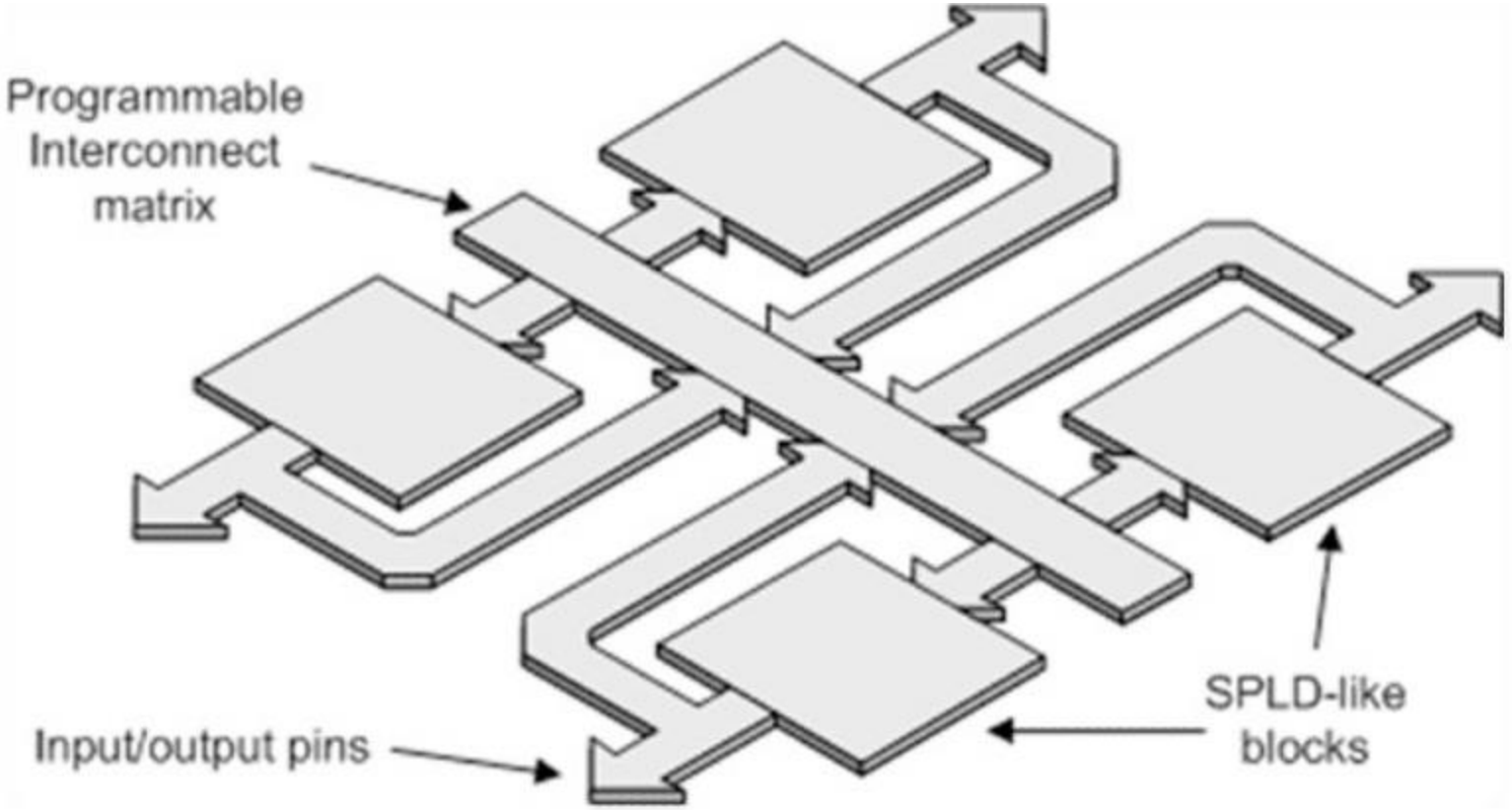
Of course there are some details
to be learnt about electronics design …

Simple PLDs (sPLDs): PROMs



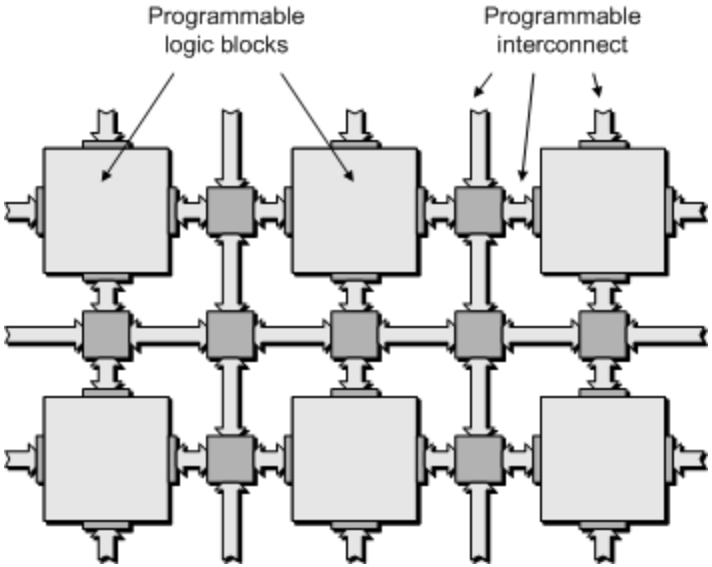
Unprogrammed PROM (Fixed AND Array, Programmable OR Array)

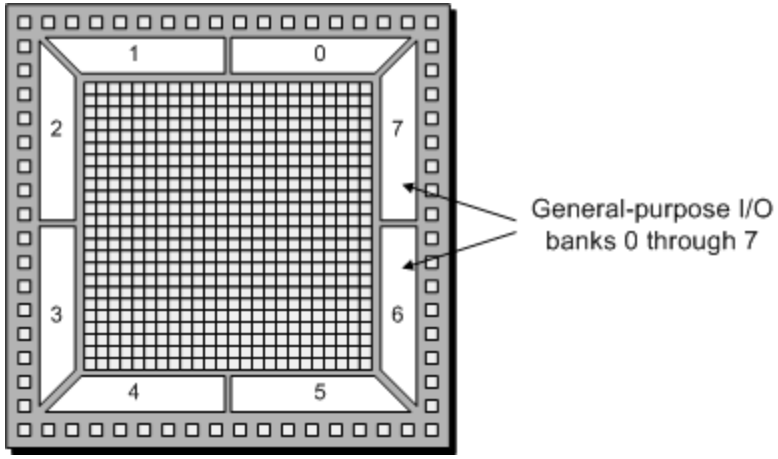
Complex PLDs (CPLDs)



Coarse grained
100's of blocks, restrictive structure
(EE)PROM based

And ……FPGA



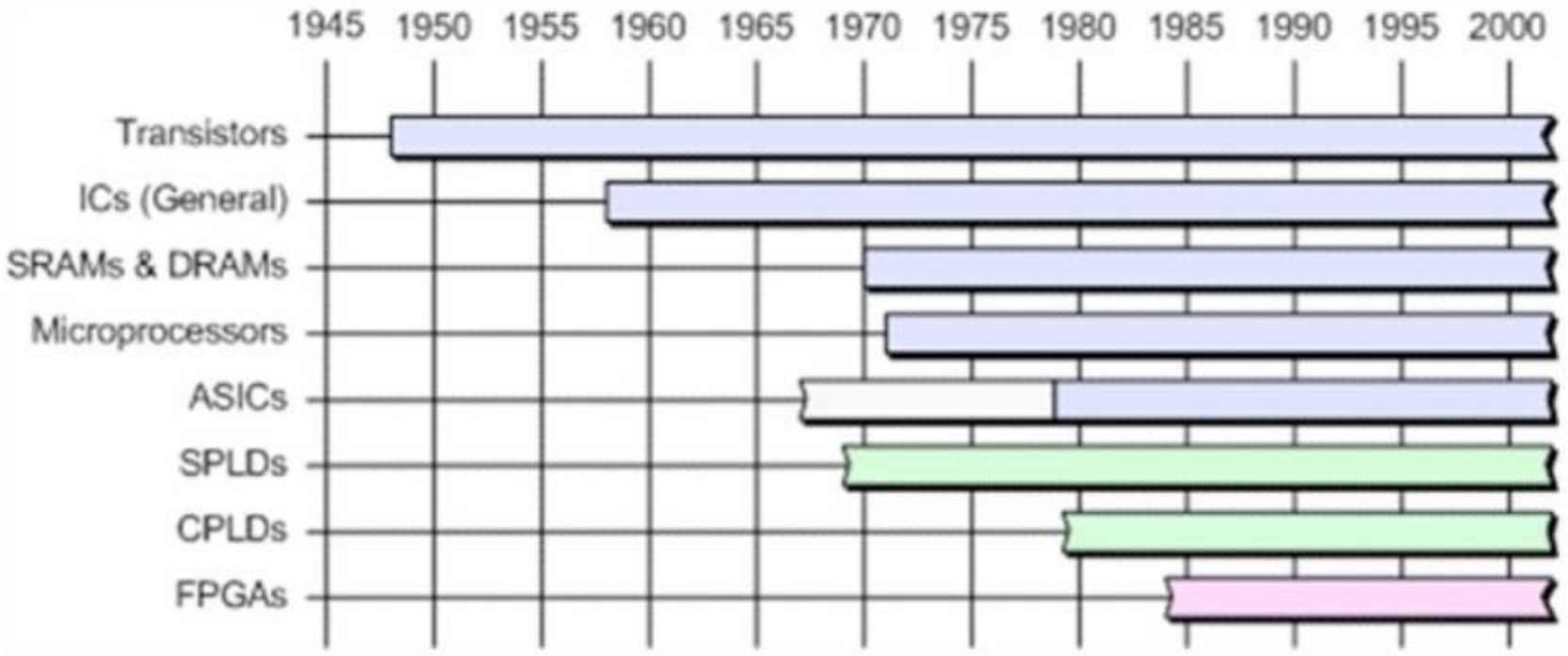


Today: Up to 1200 user I/O pins
Input and / or output
IO standard (such as LVTTL, LVDS) programmable

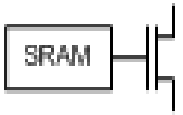
How FPGA Evolved

- The FPGA industry sprouted from programmable read-only memory (PROM) and programmable logic devices(PLDs).
- PROMs and PLDs both had the option of being programmed in batches in a factory or in the field (field programmable). However programmable logic was hard-wired between logic gates.
- Xilinx co-founders Ross Freeman and Bernard Vonderschmitt invented the first commercially viable field programmable gate array in 1985 – the XC2064.
- The XC2064 had programmable gates and programmable interconnects between gates, the beginnings of a new technology and market.
- The XC2064 boasted a mere 64 configurable logic blocks (CLBs), with two 3-input lookup tables (LUTs).

How technology and Products evolved



Summary Of Technologies

Technology	Symbol	Predominantly associated with ...
Fusible-link		SPLDs
Antifuse		FPGAs
EPROM		SPLDs and CPLDs
E^2PROM/ FLASH		SPLDs, CPLDs, and FPGAs
SRAM		FPGAs (some CPLDs)

Major Manufacturers

Xilinx

First company to produce FPGAs in 1985

- About 50% market share, today
- SRAM based CMOS devices

Altera

- About 30% market share

SRAM based CMOS devices

MicroSemi

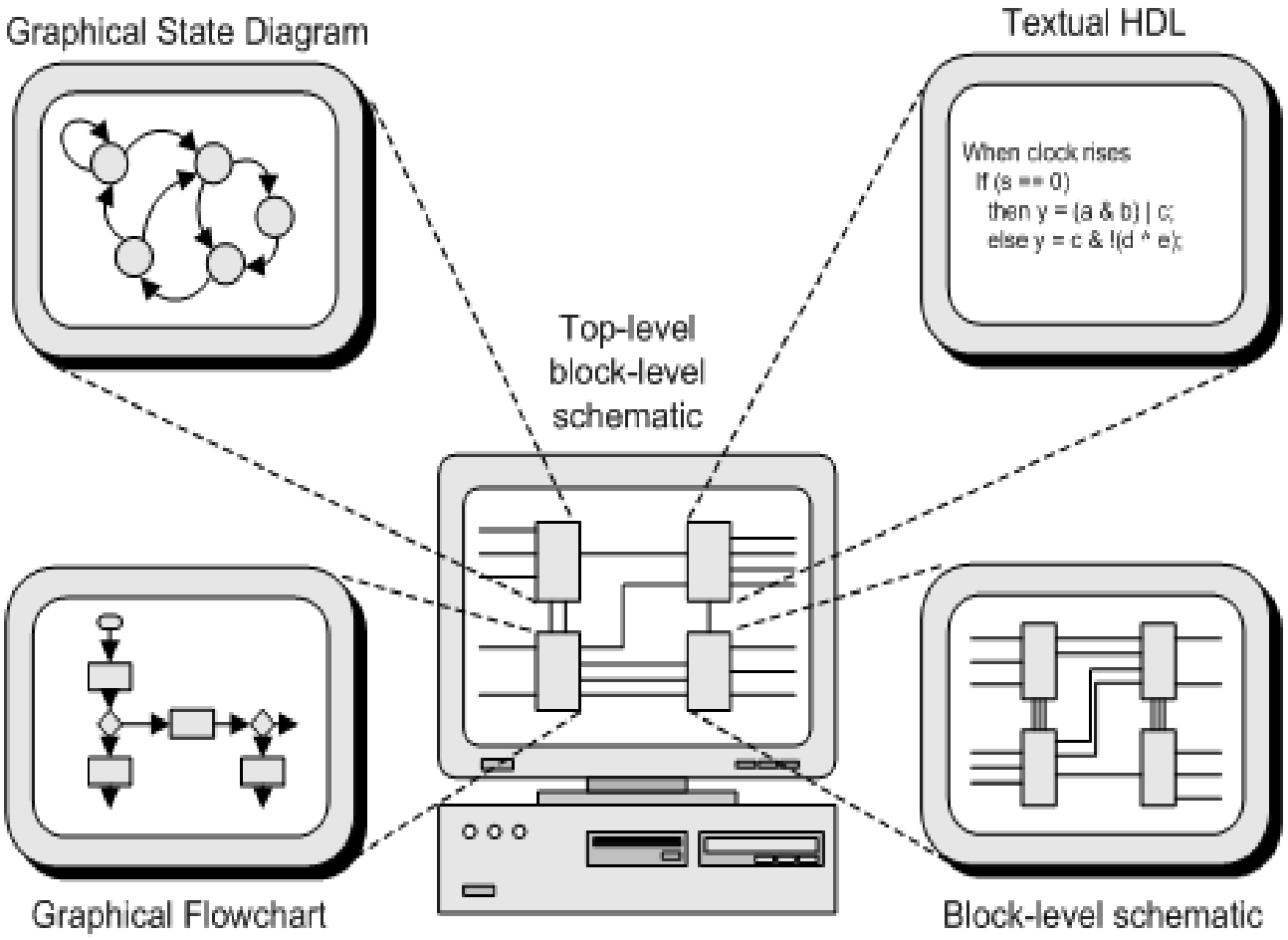
Actel

- Anti-fuse FPGAs
- Flash based FPGAs
- Mixed Signal

Lattice Semiconductor

- SRAM based with integrated Flash PROM

Development Tools



Hardware Description Language

Similar to a programming language

Common HDLs

- VHDL
- Verilog
- AHDL (Altera specific)

Newer trends

- C-like languages (handle-C)
- Labview

Example of a VHDL

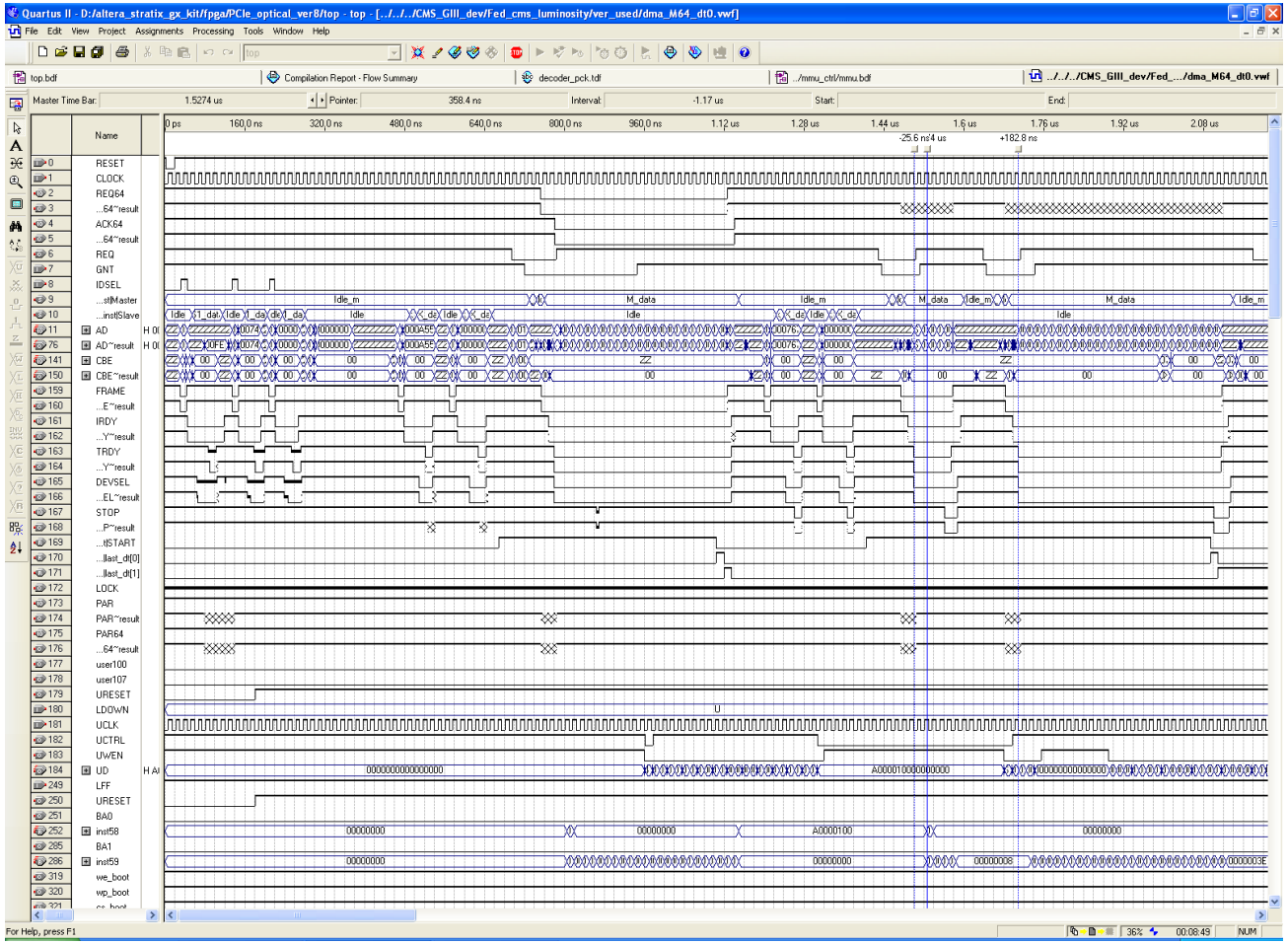
```
architecture behavioral of VMEReg is

  signal vme_en_i   : std_logic;
  signal Q : std_logic_vector(15 downto 0);

begin  -- behavioral

  vme_addr_decode : process (vme_addr, vme_en) is
    variable my_addr_vec : std_logic_vector(vme_addr'high downto 0);
    variable selected    : boolean;
  begin  -- process vme_addr_decode
    my_addr_vec := std_logic_vector( TO_UNSIGNED ( my_vme_base_address, vme_addr'high+1 ) );
    selected    := my_addr_vec(vme_addr'high downto 1) = vme_addr(vme_addr'high downto 1);
    vme_en_i <= '0' ;
    if selected then
      vme_en_i <= vme_en;
    end if;
  end process vme_addr_decode;

  reg: process (vme_clk, reset) is
  begin  -- process reg
    if reset = '1' then                 -- asynchronous reset
        Q <= init_val;
        vme_en_out <= '0';
    elsif vme_clk'event and vme_clk = '1' then  -- rising clock edge
      vme_en_out <= vme_en_i;
      if vme_en_i = '1' and vme_wr = '1' then
        Q <= vme_data;
      end if;
    end if;
  end process reg;

  data <= Q;
  vme_data_out <= Q;

end behavioral;
```

Tools from Altera

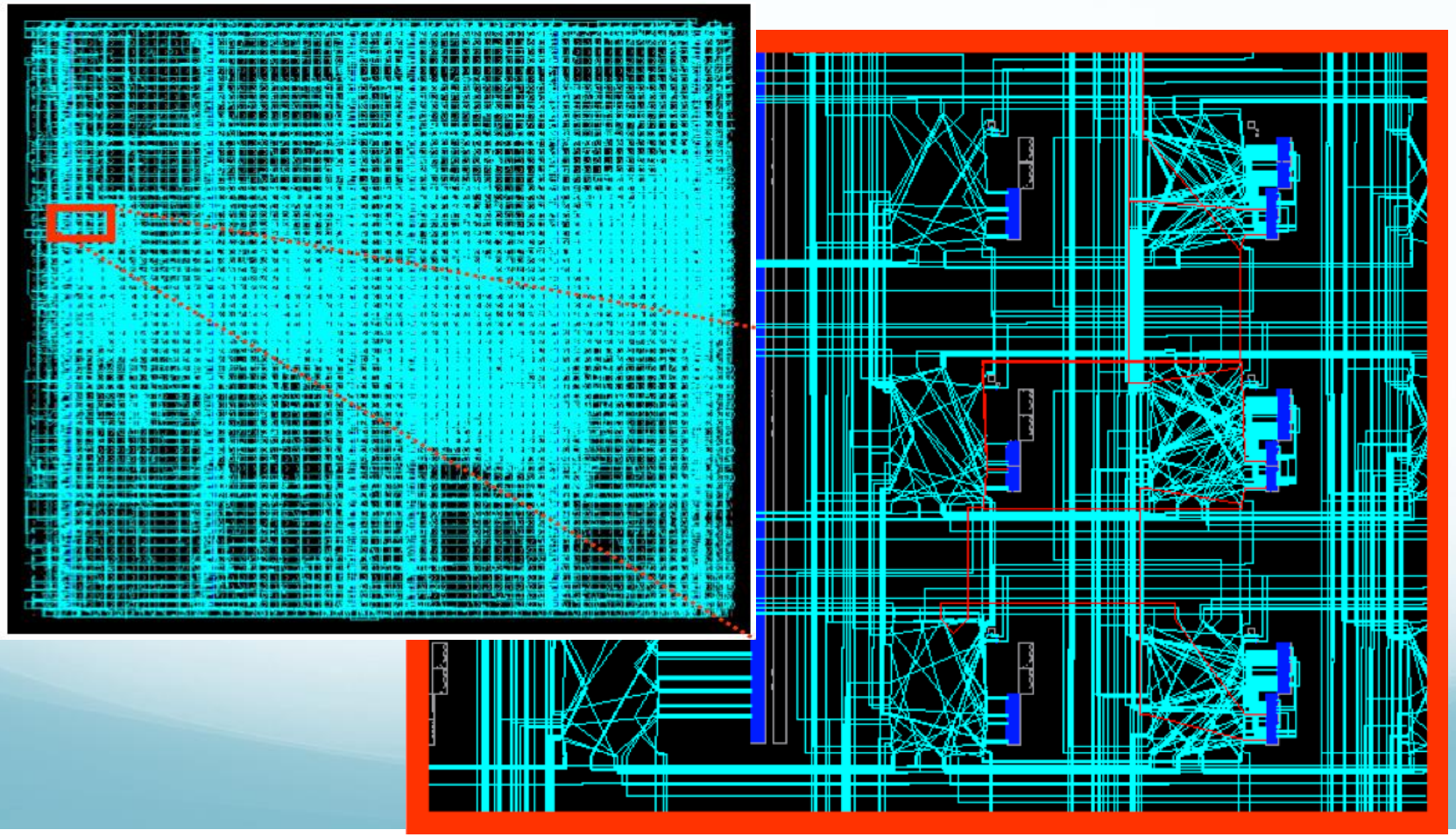
- Quartus II for different FPGA Device families (Cyclone II) used in the DE2 kit .
- ModelSim for Simulation and design verfication (funtional and timing simulation)
- Nios II IDE (to configure and Use the Nios2 processor embedded inside a Altera FPGA)

(Parallel tools for Xilinx are ISE design suite and ISE modelsim)

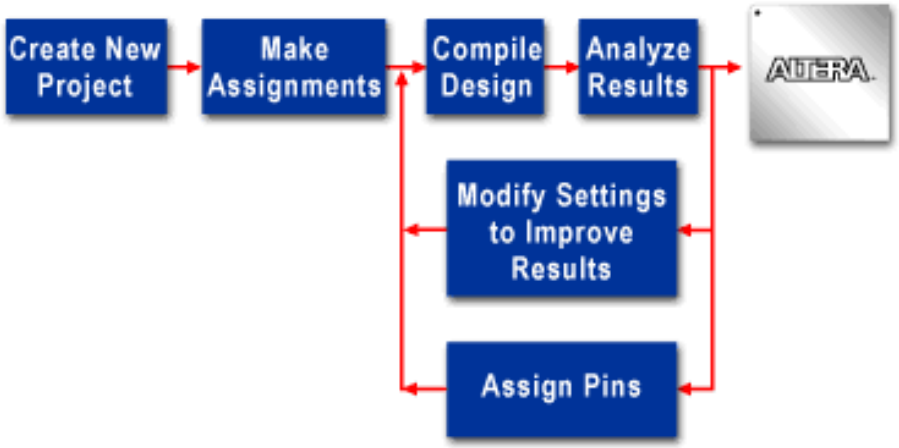
simulation


Quartus II - D:/altera_stratix_gx_kit/fpga/PCIe_optical_ver8/top - top - [../../../CMS_GIII_dev/Fed_cms_luminosity/ver_used/dma_M64_dt0.vwf]
File Edit View Project Assignments Processing Tools Window Help
top.bdf
Compilation Report - Flow Summary
decoder_pck.tdf
../mmu_ctrl/mmu.bdf
../../../CMS_GIII_dev/Fed_.../dma_M64_dt0.vwf
Master Time Bar:
Pointer:
Interval:
Start:
End:
Name
RESET
CLOCK
REQ64
ACK64
REQ
GNT
IDSEL
AD
CBE
FRAME
IRDY
TRDY
DEVSEL
STOP
PAR
PAR64
LOCK
user100
user107
URESET
LDOWN
UCLK
UCTRL
UWEN
UD
LFF
BA0
BA1
we_boot
wp_boot
Idle
Idle_m
M_data
For Help, press F1

Floorplan



How to use the tool ?



FPGA Benefits

- FPGA chip adoption across all industries is driven by the fact that FPGAs combine the best parts of ASICs and processor-based systems.
- Faster I/O response times and specialized functionality.
- Low power consumption.
- Rapid prototyping and verification without the fabrication process of custom ASIC design using the Simulator tool.
- Implementing custom functionality in a reliable manner.
- Field-upgradable eliminating the expense of custom ASIC re-design and maintenance offering great flexibility of use.

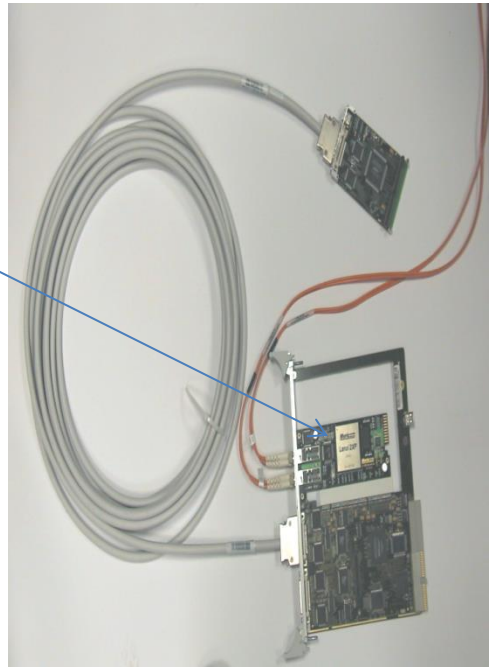
FPGAs in Data Acqusition

- Front End Elecronics
- Pedestal Subtraction
- Zero suppression
- Compression
- Custom Data Links
- eg,.Several serial LVDS links in parallel
- Upto 400 Mb/s
- Interface from custom Hardware to commercial Electronics
- VME Bus ,PCI Bus ,Myrinet e.t.c

Ex1of FPGA used in CMS FE

Front-end Readout Link
Card
1 main FPGA (Altera)

1 FPGA as PCI interface
Custom Compact PCI card
Receives 1 or 2 SLINK64



Ex2 CMS Merging Modules

These modules merge the status of all detector front-ends in CMS in order to throttle the trigger when buffers fill up.

Additionally these modules monitor all status changes of detector frontends.

1 FPGA (Altera) : PCI interface
1 FPGA (Xilinx) :

Merging logic (1 µs latency)
Monitoring logic

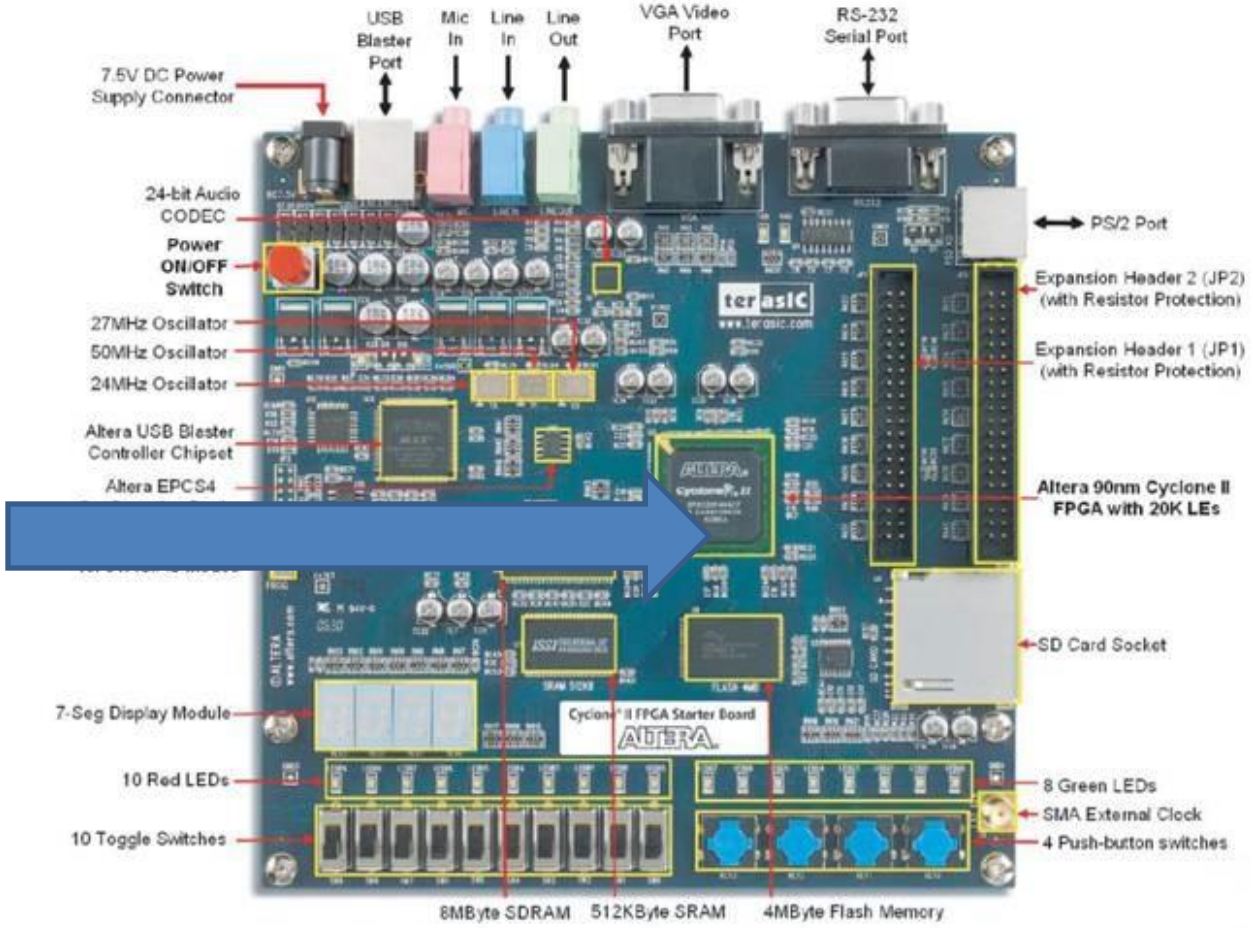
FPGAs in other domains

- Set-top boxes
- Medical imaging
- Computer vision
- Speech recognition
- Cryptography
- Bioinformatics
- Software-Defined Radio
- Aerospace
- Defense
- Digital Signal Processing
- ASIC Prototyping
- High performance computing

Trends

- Increased capacity and speed (> 1 M logic cells)
- Look-up-tables with more inputs
- High speed serial links (multiple Gb/s)
- Hard macro cores (Ethernet MAC, Memory interfaces)
- Embedded CPUs
- Sophisticated interfaces (PCI Express, …)
- Domain-specific devices
- Ultra-low-power FPGAs
- Mixed-signal FPGAs

Lab 6: Programming an FPGA



You are going to design the digital electronics inside this FPGA !

THANK YOU